100GBASE QSFP28 1310nm 10KM MPO SMF Transceiver

P/N: AE-QSFP28-PSM4

Features

- Hot-pluggable QSFP28 form factor
- Supports 103.1 Gb/s aggregate bit rate
- Power dissipation < 3.5W
- RoHS-6 compliant
- Single 3.3V power supply
- Up to 10km of Single Mode Fiber (SMF)
- 4x25G retimed electrical interface
- Parallel MPO receptacle
- I2C management interface
- Case temperature commercial range: 0°C to 70°C

Applications

- 100G PSM4 applications with FEC
- Datacenter and enterprise networking

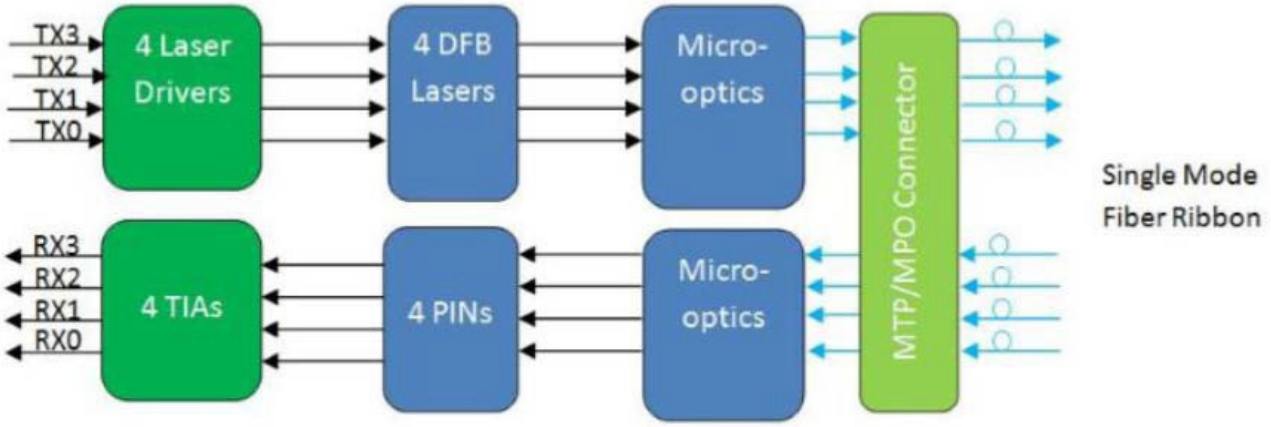
Standard

- Compliant to IEEE 802.3bm 100Gbase PSM4
- Compliant to SFF-8636
- OIF CEI-28G-VSR

Description

The 100G QSFP28 PSM4 is a parallel 100 Gbps single mode optical transceiver designed for optical communication applications. This product provides increased port density, offering four independent transmit and receive channels. Each channel operates at 25Gbps, resulting in an aggregate data rate of 100Gbps on 2km of single mode fiber. An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP28 module receptacle. The guide pins inside the receptacle ensure proper alignment. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module can be managed through the I2C two-wire serial interface.

The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 25Gb/s per channel. Figure 1 shows the functional block diagram of this product.



A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. Per MSA the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interfacebus –individual ModSelL lines for each QSFP28 module must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map. The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module

indicates a completion of the reset interrupt.

The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring are set. Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsLto a“Low” state. Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	ºC	
Relative Humidity	RH	0	-	85	%	
Power Supply Voltage	VCC	-0.5	-	3.6	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Tcase	0	-	70	ºC	Without air flow
Power Supply Voltage	VCC	3.13	3.3	3.47	V	
Power Supply Current	ICC	-		1060	mA	
Data Rate	BR		25.78125		Gbps	Each channel
Transmission Distance	TD		-	10	km	
Coupled fiber	Single mode fiber					

III. Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Wavelength range	λ0	1260	1310	1355	nm	
Total Output. Power	POUT			9.5	dBm	
Average Launch Power Per lane		-5.5		2	dBm	
Spectral Width (-20dB)	σ			1	nm	
SMSR		30			dB	

Optical Extinction Ratio	ER	3.5			dB	
Average launch Power off per lane	Poff			-30	dBm	
Output Eye Mask definition {X1，X2，X3，Y1，Y2，Y3}	{0.31,0.4,0.45,0.34,0.38,0.4}					
Receiver						
Receiver wavelength range	λin	1260		1355	nm	
Average receiver power，each lane				3.5	dBm	
Rx Sensitivity per lane	RSENS			-10	dBm	1
Input Saturation Power (Overload)	Psat	4.5			dBm	
Receiver Reflectance	Rr			-26	dB	
LOS Assert	LOSA	-18			dBm	
LOS De-Assert	LOSD			-12.0	dBm	

Notes:

*Measured with a PRBS 231 -1 test pattern, @25.78Gb/s, BER<5*10-5*

IV. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Supply Current	Icc			1060	mA	
Transmitter						
Input differential impedance	Rin	90	100	110	Ω	1
Differential data input swing	Vin,pp	190		700	mV	
Transmit Disable Voltage	VD	Vcc–1.0		Vcc	V	
Transmit Enable Voltage	VEN	Vee		Vee+ 0.8	V	2
Receiver						
Differential data output swing	Vout,pp	300		850	mV	3
LOS Fault	VLOS fault	Vcc–1.0		VccHOST	V	4
LOS Normal	VLOS norm	Vee		Vee+0.8	V	4

Notes:

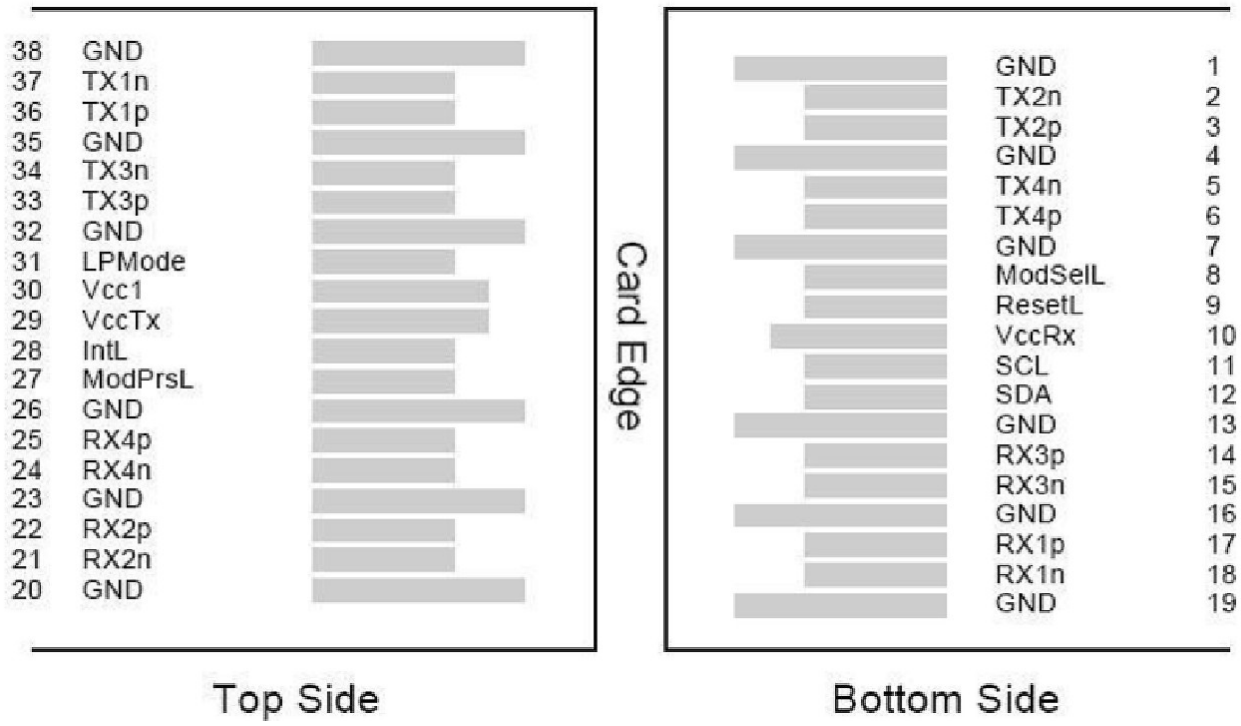
1. Connected directly to TX data input pins. AC coupled thereafter.

2. Or open circuit.

3. Into 100 ohms differential termination.

4. Loss Of Signal is LVTTL. Logic 0 indicates normal operation; logic 1 indicates no signal detected.

V. Pin Assignment



Pin	Symbol	Name/Description	Note
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	

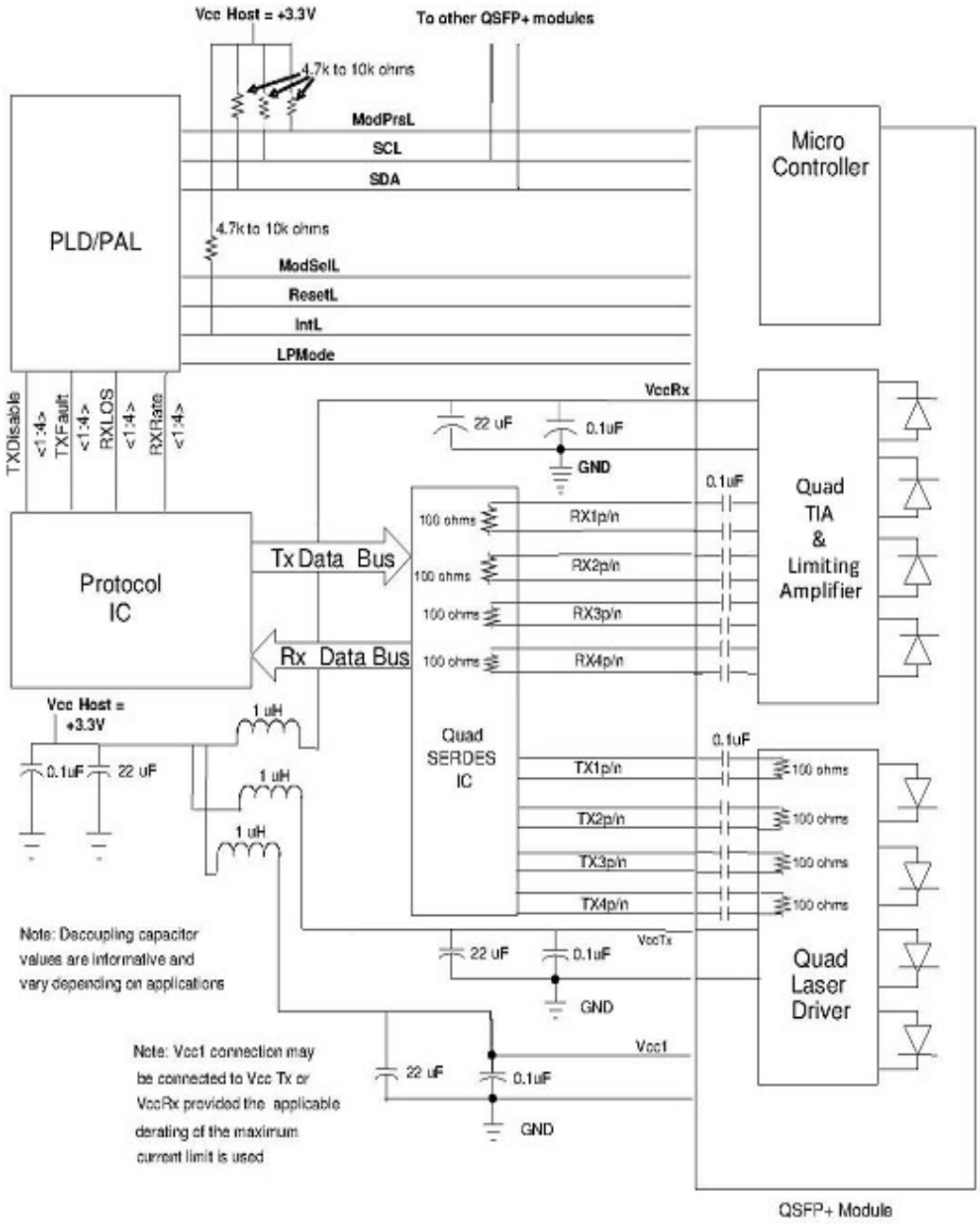
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination.

VI. Host - Transceiver Interface Block Diagram



VII. Ordering information

Part Number	Product Description
AE-QSFP28-PSM4	QSFP28, 100Gb/s, 1310nm, MPO, 10KM, DDM, 0℃ ~ +70℃