QSFP-DD 400GBASE-SR4 850nm 100m DOM Transceiver

AE-QSFPDD-SR4

Features

- Hot-pluggable QSFP-DD Form Factor
- Maximum Link Length of 100m on OM4 Fiber with FEC
- +3.3V Single Power Supply
- Power Dissipation ≤ 8W
- Operating Case Temp Commercial: 0°C to +70 °C
- Single MPO-12 APC Connector
- RoHS Compliant
- Compliant with IEEE 802.3bs Standard: 400GAUI-8 Electrical Interface

Application

- 400GBASE-SR4

Description

The AE-QSFPDD-SR4 module, MTP/MPO-12 connector, up to 100m over parallel OM4 multi-mode fiber. It is compliant to IEEE 802.3bs protocol and 400GAUI-8 standard.The 400 Gigabit Ethernet signal is carried over four parallel lanes by one wavelength per lane.And it can Support 2 x 200G-SR and 4 x 100G-SR.

Product Specifications

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	VCC3	-0.5		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Operating Humidity	RH	0		85	%	1
Control Input Voltage	VI	-0.3		V_{CC}+0.5	V	1

II. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	Tc	0		70	℃	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Dissipation	Pd			8	W	
Supply Current	ICC			2550	mA	
Pre-FEC Bit Error Ratio				2.4x10-4		
Post-FEC Bit Error Ratio				1x10-12		1
Link Distance (OM4)		2		100	m	2
Link Distance (OM3)		2		60	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

III. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Differential pk-pk Input Voltage Tolerance		900		900	mV	
Differential Termination Mismatch				10	%	
Single-ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common Mode Voltage		-350		2850	mV	

Receiver						
AC Common-mode Output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-end Eye height, differential		70			mV	
Far-end Eye height, differential		30			mV	
Far end pre-cursor ISI ratio		-4.5		2.5	%	
Differential Termination Mismatch		10			%	
Transition Time (min, 20% to 80%)		9.5			ps	
DC common mode Voltage		mV		2850	mV	

III. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Rate Per Lane	SR	53.125 ± 100 ppm			Gbd	
Modulation Format		PAM4				
Center Wavelength	CW	842		948	nm	
RMS Spectral Width	SW			0.65	dBm	1
Average Launch Power Per Lane	AOP	-4.6		4.0	dBm	
Outer Optical Modulation Amplitude (OMAouter), Each Lane (min) For max(TECQ,TDECQ)≤1.8dB	TxOMA	-2.6 4.4+max(TECQ,TDEC		3.5	dBm	

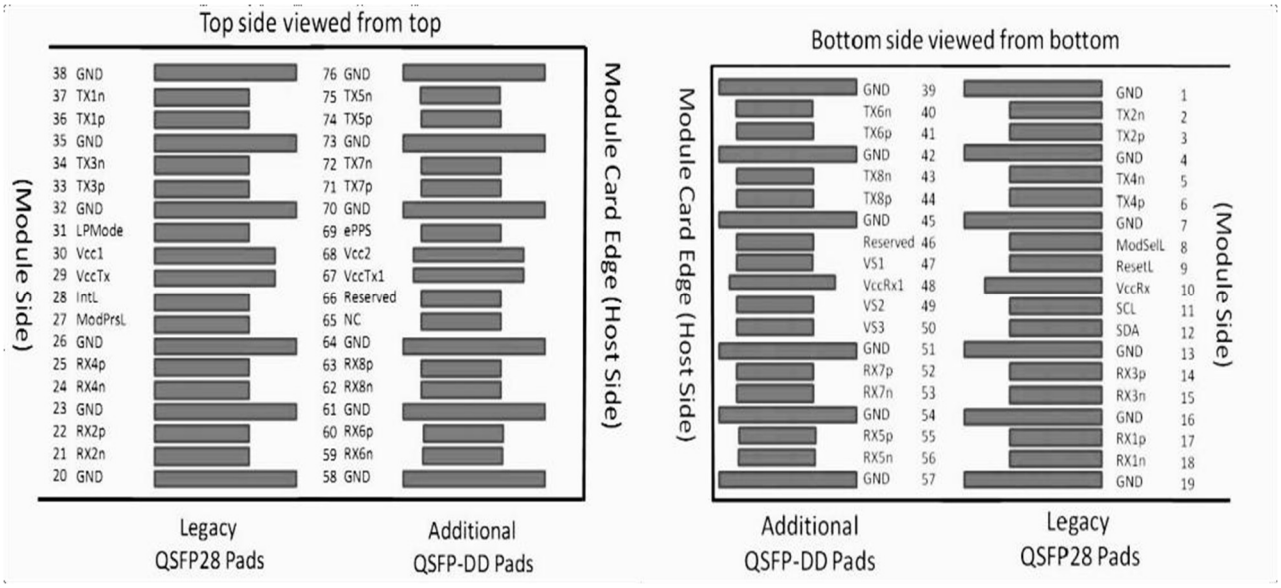
For 1.8<max(TECQ,TDECQ)≤4.4dB		Q)				
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane	TDECQ			4.4	dB	
Overshoot/Undershoot				29	%	
Transimitter Power Excursion, Each Lane				2.3	dBm	
Transition Time	Tt			17	ps	
Average Launch Power of OFF Transmitter, Each Lane	TOFF			-30	dBm	
Extinction Ratio, Each Lane	ER	2.5			dB	
Encircled Flux		≥86% at 19μm ≤30% at 4.5μm			dBm	2
Receiver						
Signaling Rate Per Lane	SR	53.125 ± 100 ppm			Gbd	
Modulation Format		PAM4				
Wavelength	W	842		948	nm	
Damage Threshold, Average Optical Power, Each Lane	DT	5			dBm	3
Average Receive Power, Each Lane	RXPx	-6.3		4	dBm	4
Receive Power (OMA) Per Lane	RxOMA			3.5	dBm	
LOS Assert	LOS_A	-15			dBm	
LOS De-assert	LOS_D			-9.2	dBm	
LOS Hysteresis	LOS_H	0.5			dB	

OMAouter of Each Aggressor Lane			3.5		dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance

Pin Descriptions



Pin Definitions

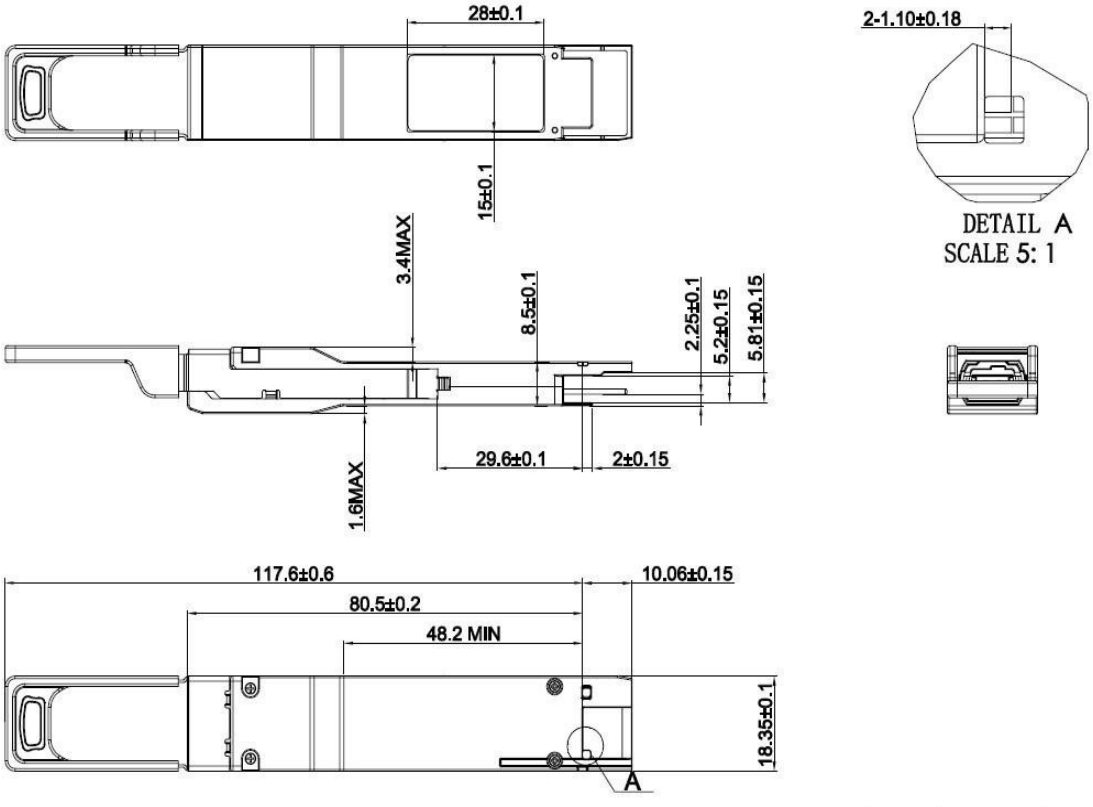
Pin	Logic	Symbol	Definition	Pin	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground

5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Select	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground

21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserved	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input

37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Mechanical Dimensions



Order Information

Part Number	Description
AE-QSFPDD-SR4	400GBASE-SR4 850nm 100m DOM QSFP-DD Transceiver MPO-16 MMF