400G QSFP-DD ER4 Lite 30km LC SMF Optical Transceiver Module

AE-QSFPDD-ER4L

Features

- Compliant with 100G Lambda MSA 400G-ER4-30 Technical Specifications
- Compliant with QSFP-DD MSA Hardware Specification
- Compliant electrical interface with IEEE 802.3bs 400GAUI-8 C2M
- Compliant with Common Management Interface Specification
- Up to 30km reach
- nWDM wavelengths: 1304.58nm, 1306.85nm, 1309.14nm and 1311.43nm
- Dual LC optical interface
- Power consumption 12W Maximum
- 3.3V Power Supply
- 0ºC to 70ºC operating case temperature
- RoHS 6 Compliant
- Hot-Pluggable

Applications

- 400G Gigabit Ethernet
- Four independent 100G-ER interconnects
- Transmission over 30km

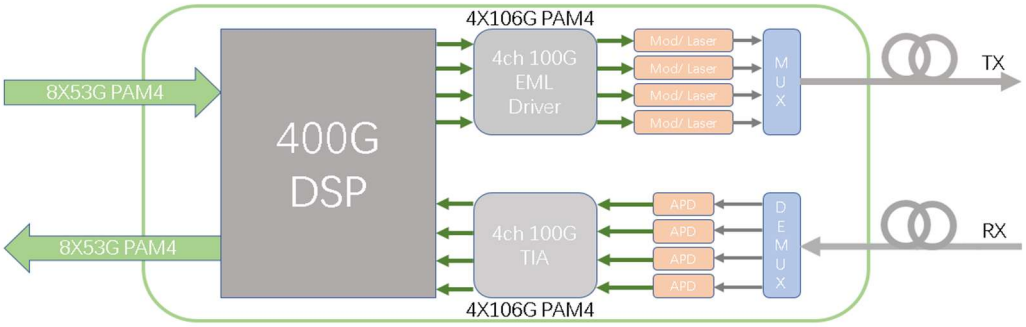
Description

The AE-QSFPDD-ER4L optical transceiver module provides high transmission density 400Gbps links over 30km single-mode fiber compliant with the 100G Lambda MSA specification. This is enabled by multiplexing four nWDM 53GBaud PAM4 (106Gbps) encoded optical signals in conjunction with advanced DSP.

The transceiver is a compact hot-pluggable QSFP-DD Type 2A form factor. The electrical interface consists of eight 26GBaud PAM4 encoded lanes providing 8x53Gbps data across the host connector compliant with 400GAUI-8 (four 100GAUI-2 lanes) and OIF CEI-56G-VSR-PAM4 standards.

The optical interface is terminated in a dual LC receptacle. Digital monitoring and control functions are supported via an I2C serial interface per the Common Management Interface Specification

Diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			3.63	A	
Power Consumption				12	W	
Case Temperature	Top	0		70	℃	
Link Distance	D			30	km	

Specifications

Transmitter Optical Specifications, EOL

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate (each Lane)		53.125 ± 100 ppm			GBd
Modulation Format		PAM4			
Wavelength	λ1	1304.06	1304.58	1305.10	nm
	λ2	1306.33	1306.85	1307.38	nm
	λ3	1308.61	1309.14	1309.66	nm
	λ4	1310.90	1311.43	1311.96	nm
Channel Polarization	Polarization of Ch0, Ch3 and Polarization of Ch1, Ch2 are orthogonal at launch				
Side-mode Suppression ratio	SMSR	30			dB
Total average launch power	TP_{AVG}			11.6	dBm
Average launch power (each Lane) [1]	P_{AVG}	0		5.6	dBm
Channel power Difference				3	dBm

Outer Optical Modulation Amplitude(each Lane)	P_{OMA}			6.4	dBm
TDECQ<1.4dB		3			
TDECQ>1.4dB		1.6+TDECQ			
Transmitter and Dispersion penalty (each Lane) [2]	TDECQ			3.5 (|CD|< 16ps/nm) 3.9 (|CD|> 16ps/nm)	dB
TECQ (each Lane)	TECQ			3.5	dB
|TDECQ-TECQ| (each Lane)				2.3 (|CD|< 16ps/nm) 2.7 (|CD|> 16ps/nm)	dB
Extinction Ratio (each Lane)		5			dB
Optical Return Loss Tolerance				15	dB
Transmitter Reflectance[3]	RL			-26	dB
Average Launch Power OFF Transmitter(each Lane)	P_{off}			-15	dBm
$RIN_{15}OMA$	RIN			-136	dB/Hz

Notes:

1. Average launch power (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. TDECQ test based on 30km fiber.
3. Transmitter Reflectance is defined looking into the transmitter.

Receiver Optical Specifications, EOL

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate (each Lane)		53.125 ± 100 ppm			GBd
Modulation Format		PAM4			
Lane Wavelength	λ	1304.06~1311.96			nm
Damage Threshold (each Lane)[1]		-2.4			dBm
Average receive power (each Lane)[2]		-14.7		-3.4	dBm
Receive Power (OMA_{outer}) (each Lane)				-2.6	dBm
Receiver Reflectance				-26	dB
Receiver sensitivity (OMAouter) (each Lane)				Max(-12.5, TECQ-13.9)	dBm

Stressed receiver sensitivity (OMAouter), (each Lane)[3]	SRS			-10	dBm
Receiver Reflectance				-26	dB
LOS Assert	LOSA	-30		-19	dBm
LOS De-assert	LOSD			-17	dBm
LOS Hysteresis	LOSH	0.5			dB
Conditions of Stress Receiver Sensitivity Test					
Stressed eye closure for PAM4 (SECQ), lane under test				3.9	dB
OMAouter of each aggressor lane				-6.4	dBm

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.
2. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3-2018.

Transmitter High Speed Electrical Characteristics

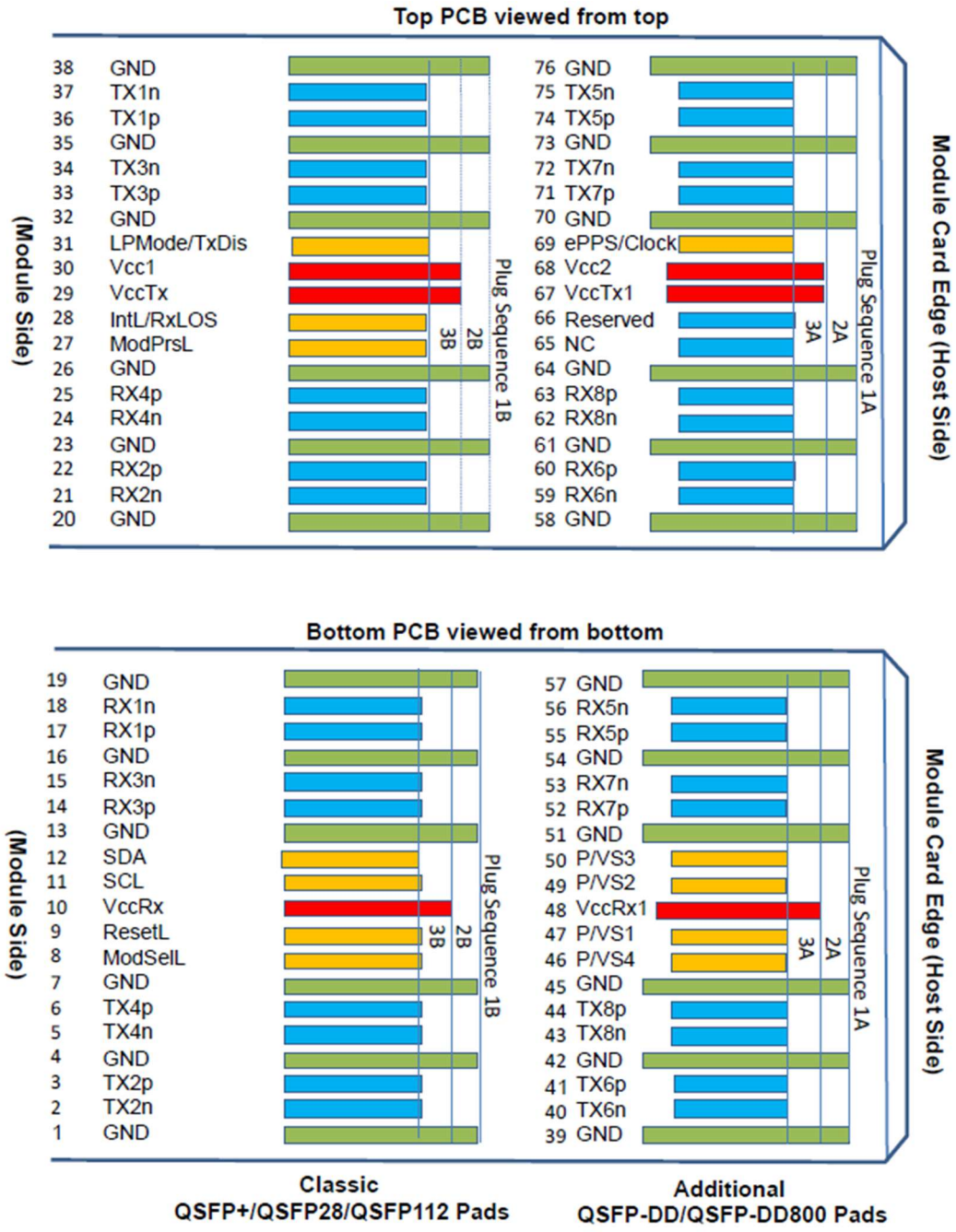
Parameter	Symbol	Min	Typ	Max	Units
Signaling rate	*Rate*	26.5625±100ppm			GBd
Differential Input Impedance	Z_d	-	100	-	Ω
Differential Input Voltage per lane	-	-	-	900	mV
Input impedance mismatch	-	-	-	10	%
Single-ended voltage tolerance range		-0.4	-	3.3	V
DC common mode voltage		-350	-	2850	mV

Receiver High Speed Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Signaling rate	*Rate*	26.5625±100ppm			GBd
DC Common mode voltage	*Vcm*	-350		2850	mV
AC common-mode output voltage RMS				17.5	mV
Differential peak-to-peak output voltage				900	mV
Near-end eye symmetry mask width (ESMW)			0.265		UI
Near-end eye height, differential		70			mV

Far-end eye symmetry mask width (ESMW)			0.2		UI
Far-end eye height, differential		30			mV
Far-end pre-cursor ISI ratio		-4.5		2.5	%
Differential termination mismatch				10	%
Transition time, 20-80%		9.5			ps

Module Connector Pad Layout



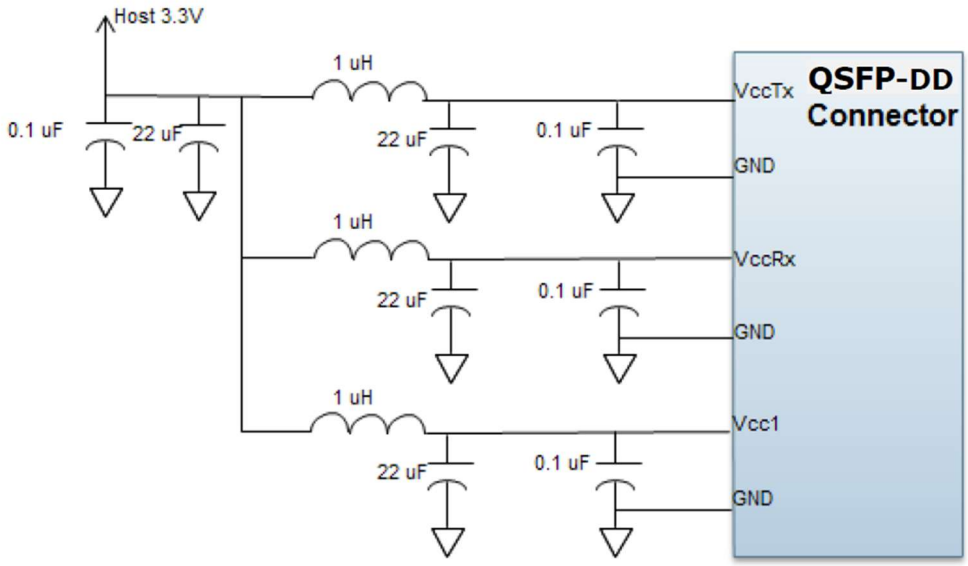
Module Connector Pad Definition

PIN	Logic	Symbol	Name / Description
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4	GND		Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7	GND		Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10	VccRx		+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13	GND		Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16	GND		Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19	GND		Ground
20	GND		Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23	GND		Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26	GND		Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt

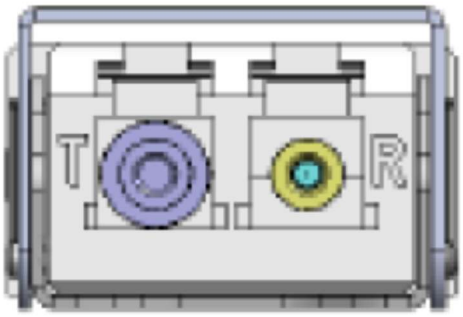
29	VccTx		+3.3V Power supply transmitter
30	Vcc1		+3.3V Power supply
31	LVTTL-I	LPMode	Low Power mode
32	GND	Ground	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35	GND		Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38	GND		Ground
39	GND	Ground	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input
42	GND		Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input
45	GND		Ground
46	Reserved		For future use
47	VS1		Module Vendor Specific 1
48	VccRx1		3.3V Power Supply
49	VS2		Module Vendor Specific 2
50	VS3		Module Vendor Specific 3
51	GND		Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54	GND		Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57	GND		Ground
58	GND		Ground

59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61	GND		Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64	GND		Ground
65	NC		No Connect
66	Reserved		For future use
67	VccTx1		3.3V Power Supply
68	Vcc2		3.3V Power Supply
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input
70	GND		Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input
72	CML-I	Tx7n	Transmitter Inverted Data Input
73	GND		Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input
75	CML-I	Tx5n	Transmitter Inverted Data Input
76	GND		Ground

Power Supply Filtering



Optical Interface



The port mapping is as follows if work in 4x100G mode:

- Electrical data Tx1/Rx1 and Tx2/Rx2 map to optical lane L1 (λ1)
- Electrical data Tx3/Rx3 and Tx4/Rx4 map to optical lane L2 (λ2)
- Electrical data Tx5/Rx5 and Tx6/Rx6 map to optical lane L3 (λ3)
- Electrical data Tx7/Rx7 and Tx8/Rx8 map to optical lane L4 (λ4)

Low Speed Electrical Hardware Signals Description

Electrical interface: All signal interfaces are compliant with the QSFP28 MSA specifications. The high-speed DATA. In addition to the 2-wire serial interface the module has the following low speed signals for control and status: ModSelL, ResetL,LPMode, ModPrsL, IntL.

ModSelL: The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

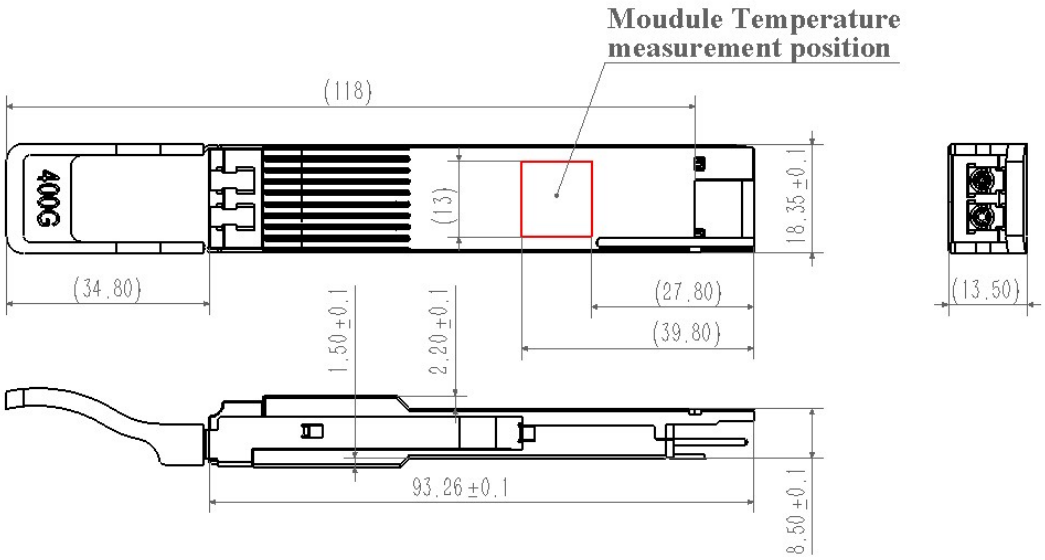
ResetL: The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode: LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode, see CMIS 4.0 Chapter 6.3.1.3.

ModPrsL: ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL: IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Mechanical Dimensions



Digital Diagnostic

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-3	3	dB	Each lane
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-3	3	dB	Each lane

Order Information

Part Number	Description
AE-QSFPDD-ER4L	QSFP-DD 400G ER4L 1310nm 30KM DOM LC