800GBASE-SR8 QSFP-DD 850nm 50m MTP/MPO-16 DOM Transceiver

AE-QDD800-SR8

Features

- Hot-pluggable QSFP-DD Form Factor
- VCSEL Transmitter and PIN PD Receiver
- Support 850Gb/s Aggregate Bit Rate
- Compliant with IEEE 802.3-2022: 8x100GBASE-SR1 Optical Interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M Electrical Interface
- C Compliant with QSFP-DD HW Specification Rev 6.3 type 2A Housing
- Compliant with CMIS Rev 5.0
- Case Operating Temperature 0°C to 70°C
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS Compliant)
- Class 1 Laser

Applications

- 800G Ethernet

Description

The 800GBASE-SR8 QSFP-DD Optical Transceiver Module supports up to 50m link lengths over multi-mode fiber (MMF) via MTP/MPO- 16 connectors. This transceiver is compliant with IEE802.3ck, CMIS 5.0 and QSFP-DD MSA standards. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters. It is suitable for 800G Ethernet.

Product Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	℃
Supply Voltage	VCC		3.6	V
Relative Humidity (Non-condensing)	RH	5	85	%
Data Input Voltage Differential	IVDIP-VDINI		1	V
Control Input Voltage	V_I	-0.3	V_{CC}+0.3	V

Control Output Current	I_O	-20	20	mA

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	TOPR	0		70	℃	1
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	ICC_IP			TBD	mA	
Sustained Peak Current at Hot Plug	ICC_SP			TBD	mA	
Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Maximum Power Dissipation	PD			TBD	W	
Maximum Power Dissipation, Low Power Mode	PDLP			1.5	W	
Signalling Speed Per Lane	DRL		53.125		GBd	
Control Input Voltage High	VIH	VCC*0.7		VCC+0.3	V	
Control Input Voltage Low	VIL	-0.3		VCC*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
Operating Distance		2		50	m	1

Note:

1. 0.5 m to 30 m for OM3, 0.5 m to 50 m for OM4 and OM5, with FEC.

Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter						
Signaling Rate, Each Lane (Range)		53.125 ± 100 ppm			GBd	
Wavelength	λC	840		860	nm	
RMS Spectral Width	RMS			0.6	dB	1
Average Launch Power, Each Lane	AOPL	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMAouter), Each Lane	OMAouter	-2.6 -		3.5	dBm	

for Max (TECQ, TDECQ) <= 1.8 dB for 1.8 < Max (TECQ, TDECQ) <= 4.4 dB		4.4+max (TECQ, TDECQ)				
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane	TDECQ			TBD	dB	
Transmitter Eye Closure for PAM4 (TECQ), Each Lane	TECQ			TBD	dB	
Over/Under-shoot				29	%	
Transmitter Power Excursion, Each Lane				2.3	dBm	
Average Launch Power of OFF Transmitter, Each Lane	TOFF			-30	dBm	
Extinction Ratio, Each Lane	ER	2.5			dB	
Transmitter Transition Time, Each Lane	Tr			17	ps	
RIN14OMA	RIN			-132	dB/Hz	
Optical Return Loss to Lerance	ORL			14	dB	
Encircled Flux		>=86% at 19μm <=30% at 4.5μm				
Receiver						
Signaling Rate, Each Lane (Range)		53.125 ± 100 ppm			GBd	
Wavelength	λC0	840		860	nm	
Damage Threshold, Each Lane	AOPD	5			dBm	
Average Receive Power, Each Lane	AOPR	-6.4		4	dBm	
Receive Power (OMAouter), Each Lane	OMAR			3.5	dBm	
Receiver Reflectance	RR			-15	dB	
Receiver Sensitivity (OMAouter) for TECQ < 1.4 dB for 1.4 dB <=TECQ<=3.4 dB	SOMA			–4.6 –6.4 + TECQ	dBm	
Stressed Receiver Sensitivity (OMAouter), Each Lane	SRS			-2	dBm	2
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test	SECQ		4.4		dB	
OMAouter of Each Aggressor Lane			3.5		dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Measured with conformance test signal at TP3 for the BER = 2.4x10-4

High Speed Electrical Signals

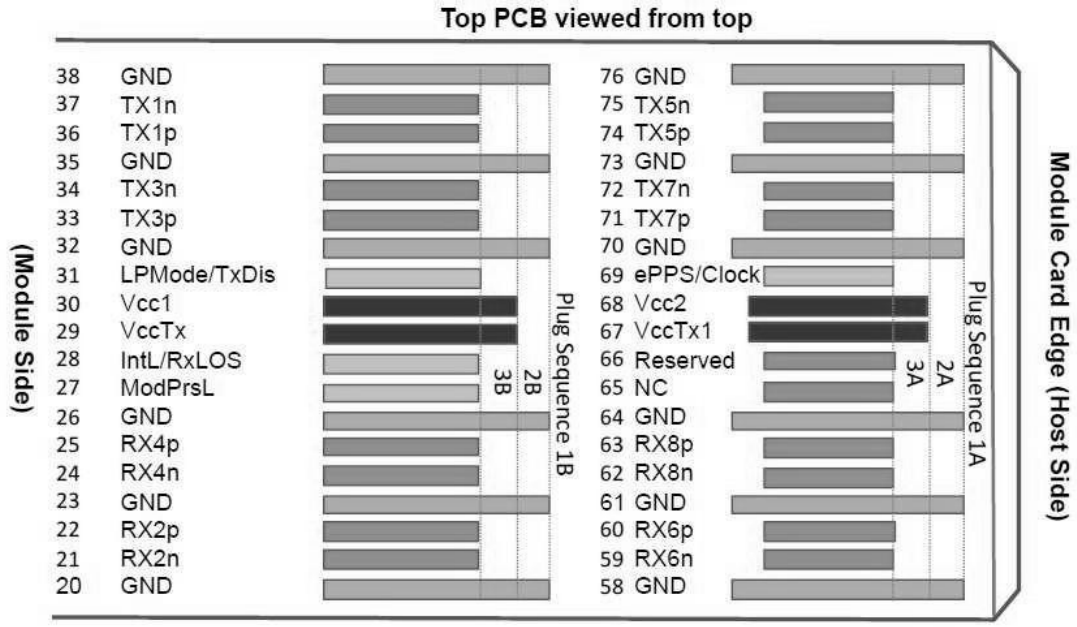
Parameter	Symbol	Min.	Typ.	Max.	Unit
Transmitter (Module Input, TP1)					
Differential Pk-pk Input Voltage Tolerance (TP1a)		750			mV
Peak-to-peak AC Common-mode Voltage Tolerance:					
Low-frequency, VCMLF		32			mV
Full-band, VCMFB		80			mV
Differential-mode to Common-mode Return Loss	RLcd	802.3ck 120G-2			dB
Effective Return Loss	ERL	8.5			dB
Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential Termination Mismatch				10	%
Single-ended Voltage Tolerance Range		-0.4		3.3	V
DC Common-mode Voltage Tolerance		-0.35		2.85	V
Receiver (Module Output, TP4)					
Peak-to-peak AC Common-mode Voltage:					
Low-frequency, VCMLF				32	mV
Full-band, VCMFB				80	mV
Differential Peak-to-peak Output Voltage:					
Short Mode				600	mV
Long Mode				845	mV
Eye Height	EH	15			mV
Vertical Eye Closure	VEC			12	dB
Common-mode to Differential-mode Return Loss	RLDC	802.3ck 120G-1			dB
Effective Return Loss	ERL	8.5			dB
Differential Termination Mismatch				10	%
Transition Time		8.5			ps

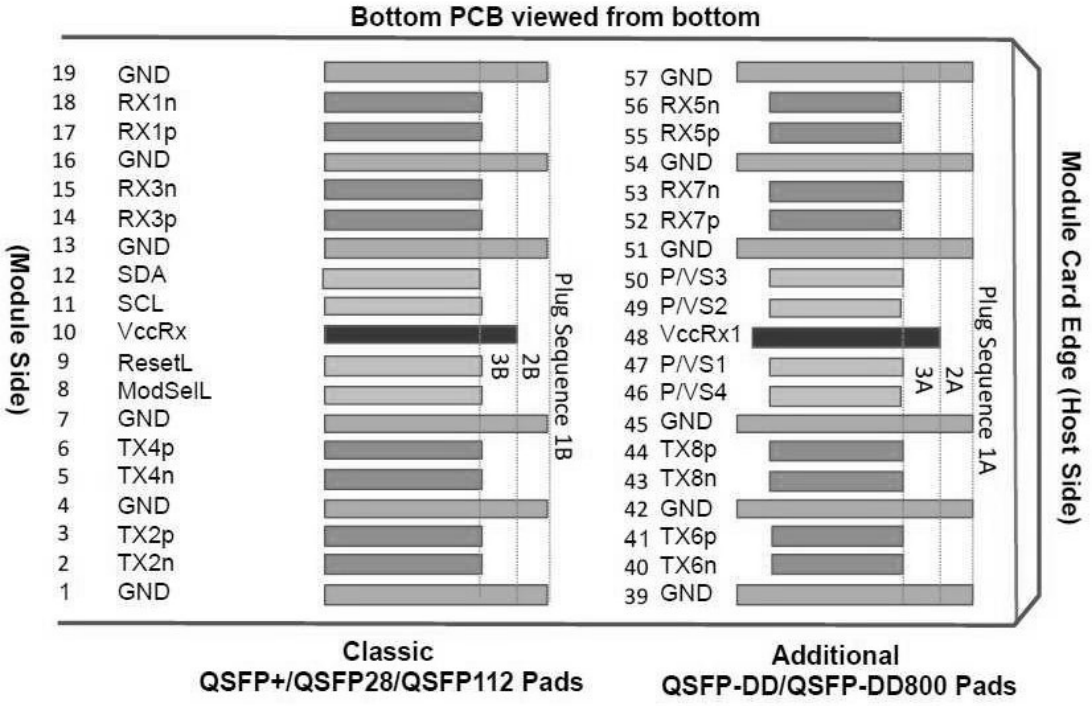
DC Common-mode Voltage Tolerance		-0.35		2.85	V

Low Speed Electrical Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit
Module Output SCL and SDA	VOL	0		0.4	V
Module Input SCL and SDA	VIL	-0.3		VCC*0.3	V
	VIH	VCC *0.7		VCC +0.5	V
InitMode, ResetL and ModSelL	VIL	-0.3		0.8	V
	VIH	2		VCC + 0.3	V
IntL	VOL	0		0.4	V
	VOH	VCC - 0.5		VCC + 0.3	V

Pin Definition





Pin Description

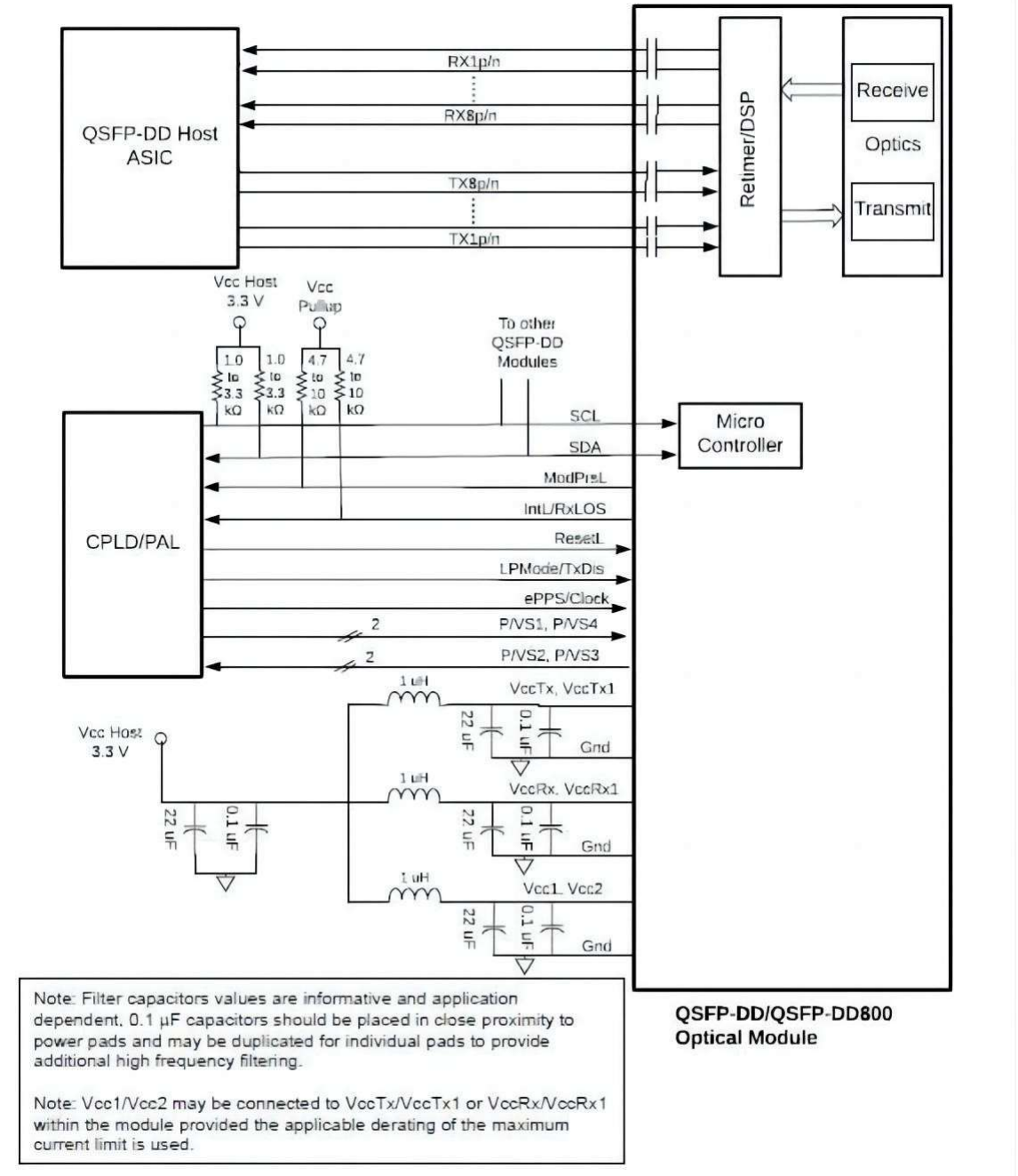
Pin	Logic	Symbol	Description
1		GND	Ground
2	CML-I	TX2n	Transmitted Inverted Data Input
3	CML-I	TX2p	Transmitted Non-Inverted Data Input
4		GND	Ground
5	CML-I	TX4n	Transmitted Inverted Data Input
6	CML-I	TX4p	Transmitted Non-Inverted Data Input
7		GND	Ground
Pin	Logic	Symbol	Description
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VCC RX	+3.3 VDC Power Supply Receiver
11	LVCMOS-I/O	SCL	TWI Serial Interface Clock
12	LVCMOS-I/O	SDA	TWI Serial Interface Data
13		GND	Ground
14	CML-O	RX3p	Receiver Non-Inverted Data Output

15	CML-O	RX3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	RX1p	Receiver Non-Inverted Data Output
18	CML-O	RX1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	RX2n	Receiver Inverted Data Output
22	CML-O	RX2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	RX4n	Receiver Inverted Data Output
25	CML-O	RX4p	Receiver Non-Inverted Data Output
Pin	Logic	Symbol	Description
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL/RXLOS	Interrupt/Optional RxLOS
29		VCC TX	+3.3 V Power Supply Transmitter
30		VCC1	+3.3 V Power Supply
31	LVTTL-I	LPMode/TX Dis	Low Power Mode/Optioanl TX Disable
32		GND	Ground
33	CML-I	TX3p	Transmitted Non-Inverted Data Input
34	CML-I	TX3n	Transmitted Inverted Data Input
35		GND	Ground
36	CML-I	TX1p	Transmitted Non-Inverted Data Input
37	CML-I	TX1n	Transmitted Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	TX 6n	Transmitter Inverted Data Input
41	CML-I	TX 6p	Transmitter Non-inverted Data Input
42		GND	Ground
43	CML-I	TX 8n	Transmitter Inverted Data Input

Pin	Logic	Symbol	Description
44	CML-I	TX 8p	Transmitter Non-inverted Data Input
45		GND	Ground
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1
48		VCC RX1	3.3V Power Supply
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3
51		GND	Ground
52	CML-O	RX 7p	Receiver Non-inverted Data Output
53	CML-O	RX 7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	RX 5p	Receiver Non-inverted Data Output
56	CML-O	RX 5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	RX 6n	Receiver Inverted Data Output
60	CML-O	RX 6p	Receiver Non-inverted Data Output
61		GND	Ground
Pin	Logic	Symbol	Description
62	CML-O	RX 8n	Receiver Inverted DataOutput
63	CML-O	RX 8p	Receiver Non-inverted Data Output
64		GND	Ground
65		NC	Not Connected
66		Reserved	
67		VCCTX1	3.3V Power Supply
68		VCC2	3.3V Power Supply
69	LVCMOS-I	ePPS/Clock	1PPS PTP Clock or Reference Clock Input
70		GND	Ground
71	CML-I	TX7p	Transmitter Non-inverted Data Input

72	CML-I	TX7n	Transmitter Inverted Data Input
73		GND	Ground
74	CML-I	TX5p	Transmitter Non-inverted Data Input
75	CML-I	TX5n	Transmitter Inverted Data Input
76		GND	Ground

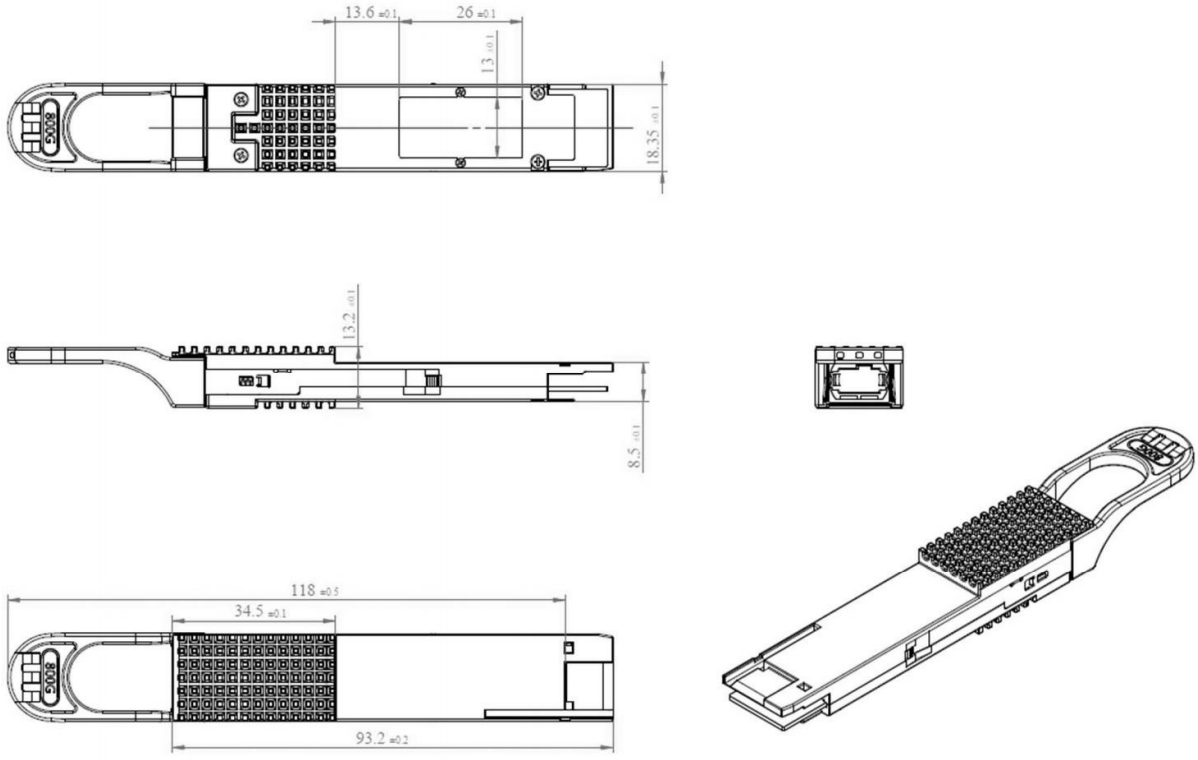
Principle Diagram



Digital Diagnostic Monitoring Specifications

Parameter	Range	Accuracy	Unit
Temperature	0 to 70	± 3	℃
Voltage	0 to VCC	0.1	V
TX Bias Current (Each Lane)	0 to 15	10%	mA
TX Output Power (Each Lane)	-4.6 to +4	± 3	dB
RX Receive Power (Each Lane)	-6.4 to +4	± 3	dB

Mechanical Dimensions



Order Information

Part Number	Description
QDD-DR8-800G	800GBASE DR8 QSFP-DD Transceiver, MTP/MPO-16, 500m over SMF