400G QSFP-DD FR4 Optical Transceiver

P/N: AE-QSFPDD-FR4

This product is a 400Gb/s QSFP-DD optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission. on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.
The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. Host FEC is required to support up to 2km fiber transmission.
The transceiver is based on proprietary AERECH Network, using surface mounted opto-electronic devices with no free space elements. The unique design of the optical engine facilitates unparalleled compactness while maintaining Telcordia robustness.

Applications

400G BASE-FR4 Ethernet
Data Center Interconnect
Infiniband Interconnect
Enterprise Networking

Features

Compliant to QSFP-DD MSA
4 CWDM lanes MUX/DEMUX design
100G Lambda MSA 400G-FR4 Specification compliant
Maximum power consumption 10W

General Description

Compliant with IEEE Std 802.3cd
Compliant with 400G-FR4 optical specifications
Compliant with QSFP-DD MSA
Compliant with CMIS4.0 Management interface specifications
8x53.125Gb/s electrical interface (400GAUI-8)
Up to 2km transmission on single mode fiber (SMF) with FEC
Single +3.3V power supply
Case temperature range: 0 ~ +70℃
Maximum power consumption 10W
Duplex LC connector
RoHS complaint

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature Range	T_{STG}	-40	+85	°C
Supply Voltage	V_{CC}	0	4	V
Relative Humidity	RH	10% to 90% non-condensing		

Operating Conditions

Parameter	Symbol	Min	Max	Units
Case Temperature- Operating	T_{CASE}	0	70	°C
Supply Voltage	Vcc	3.14	3.46	V
Power Consumption	P_{DISS}		10	W
Pre-FEC Bit Error Ratio			$2.4x10^{-4}$	
Link Distance	2		2000	M

Wavelength Lane Assignments

Transmitter Parameter	Lane	Min	Typical	Max	Units
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm

Transmitter Optical Specifications

Transmitter Parameter	Lane	Min	Typical	Max	Units
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm
Average launch Power per lane		-3.3		3.5	dBm
Total Average launch power				9.3	dBm
Outer Optical Modulation Amplitude (OMAouter), each lane		-0.3		3.7	dBm
Difference in launch power between any two lanes (OMAouter)				4	dB
Average Launch Power per Lane @ TX Off State				-20	dBm
Launch Power in OMAouter minus TDECQ, each Lane for ER ⩾ 4.5dB for ER < 4.5dB		 -1.7 -1.6			dBm
Transmitter and Dispersion Eye Closure for PAM4, each Lane				3.4	dB
Extinction Ratio		3.5			dB
Relative Intensity Noise (OMA)				-136	dB/Hz
Side-Mode Suppression Ration (SMSR)		30			dB
Optical Return Loss Tolerance				17.1	dB
Transmitter Reflectance				-26	dB
Transmitter Output Power Monitoring Accuracy		-3		3	dB
TDECQ – 10*log10(Ceq), each Lane				3.4	dB
Transmitter transition time				17	ps

Receiver Optical Specifications

Receiver Parameter	Lane	Min	Typical	Max	Units
Lane Wavelength Range	Lane 0	1264.5	1271	1277.5	nm
	Lane 1	1284.5	1291	1297.5	nm
	Lane 2	1304.5	1311	1317.5	nm
	Lane 3	1324.5	1331	1337.5	nm
Damage Threshold		4.5			dBm
Average Receive Power, each lane		-7.3		3.5	dBm
Receiver Power, each lane (OMA)				3.7	dBm
Receiver Reflectance				-26.0	dB
Difference in receive Power between any Two Lanes(OMA_{outer})				4.1	dBm
Receiver Sensitivity each lane (OMA_{outer})				max(-4.6,SECQ-6.0)	dBm
Stressed Receiver Sensitivity (OMA_{outer}), each				-2.6	dBm
Stressed Conditions for Stress Receiver Sensitivity					
Stressed Eye Closure for PAM4 (SECQ),Lane under Test			3.4		dB
SECQ – 10*log10(Ceq), lane under test			3.4		dB
OMAouter of each Aggressor Lane			1.5		dBm

High Speed Electrical Specifications

Parameter	Min	Typical	Max	Units	Notes
Receiver electrical output characteristics at TP4					
Signaling rate per lane		26.5625		GBd	
AC common-mode output voltage(RMS)		-	17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265		UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2		UI	
Far-end Eye height, differential	30			mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	9.5 - 0.37f			dB	0.01 – 8 GHz
	4.75 -7.4log 10 (f/14)			dB	8 – 19 GHz
Common to differential mode conversion return loss	22-20(f/25.78)			dB	0.01 -12.89GHz
	15 -6log 10 (f/25.78)			dB	12.89 – 19 GHz
Differential termination mismatch			10	%	
Transition time (min, 20% to 80%)	9.5			ps	
DC common mode voltage	-350		2850	mV	
Transmitter electrical input characteristics at TP1					
Signaling rate, per lane		26.5625		GBd	
Differential pk-pk input voltage tolerance	900			mV	
Differential input return loss	9.5 - 0.37f			dB	0.01 – 8 GHz
	4.75 -7.4log 10 (f/14)			dB	8 – 19 GHz
Differential to common mode input return loss	22-20(f/25.78)			dB	0.01 -12.89GHz
	15 -6log 10 (f/25.78)			dB	12.89 – 19 GHz
Differential termination mismatch			10	%	
Module stressed input test	Per Section 120E.3.4.1, IEEE802.3bs				
Single-ended voltage tolerance range	-0.4		3.3	V	
Common-mode voltage	-350		2850	mV	

Receiver Output Power Thresholds for Loss of Signal (LOS)

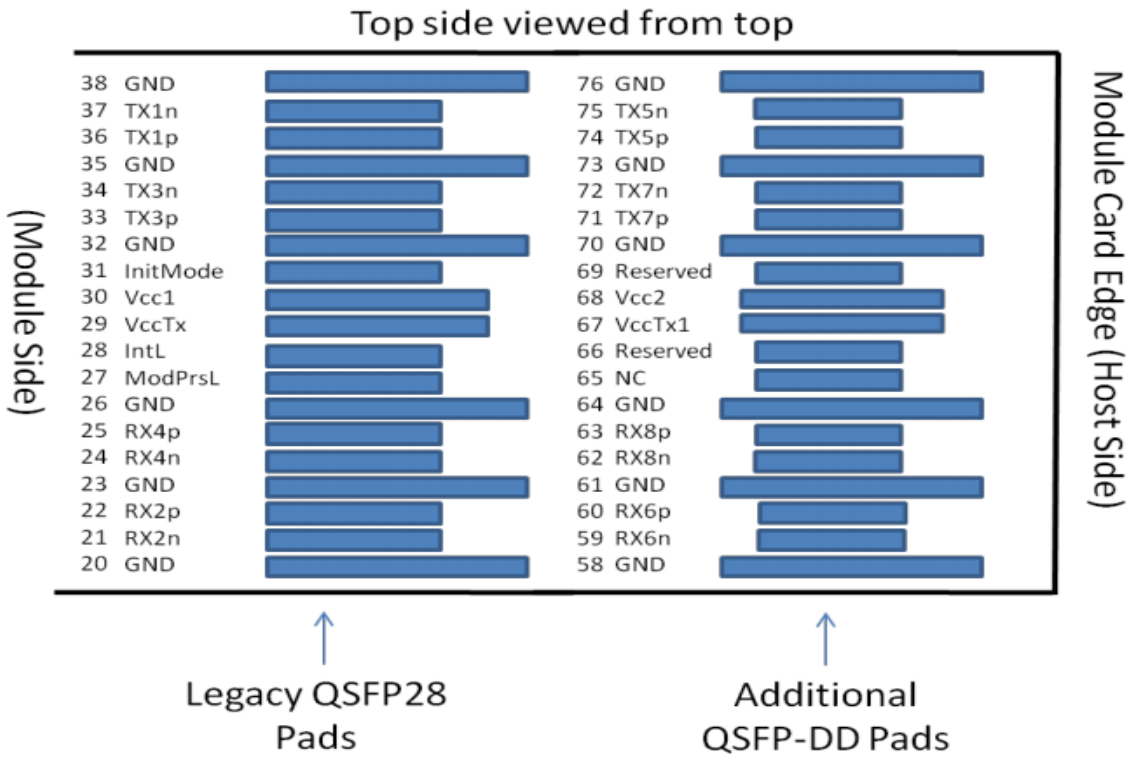
Parameter	Min	Typical	Max	Units
RX_LOS_Assert Min/Max	-20.0			dBm
RX_LOS_De-Assert Min/Max			-10.3	dBm
RX_LOS_Hysteresis	0.5			dB

Digital Diagnostic Monitoring Specifications

Parameters	Unit	Specification
Temperature Monitor absolute error	degC	± 3
Voltage Monitor absolute error	%	± 5
I_bias Monitor absolute error	%	± 10
Received Power (Rx) Monitor absolute error	dB	± 3.0
Transmit Power (Tx) Monitor absolute error	dB	± 3.0

QSFP-DD Edge Connector and Pinout Description

The electrical pinout of the QSFP-DD module is shown in Figure 2 below.



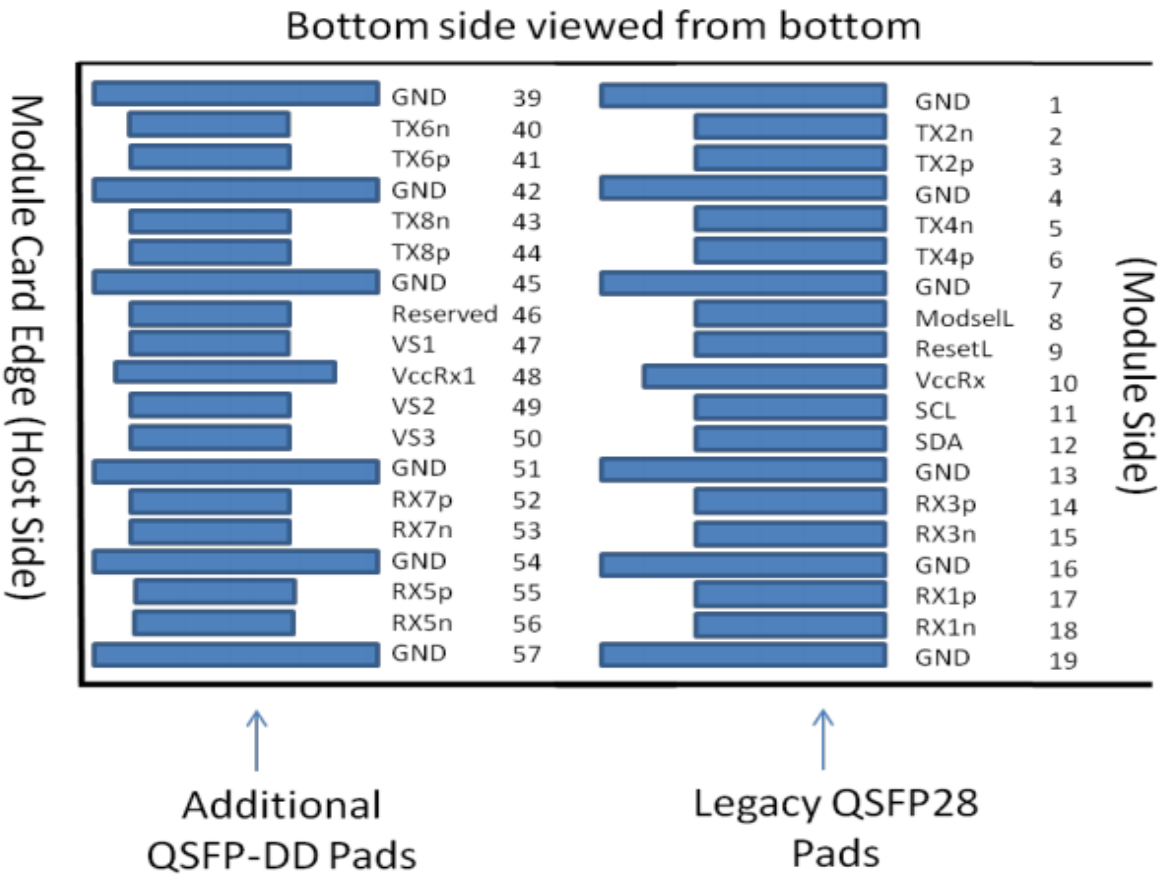


Figure 1. Host PCB QSFP-DD pad assignment top view

Pin No.	Symbol	Description	Note
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	Init Mode	Initialization mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Ground	1

39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data output	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data output	
45	GND	Ground	1
46	Reserved	For Future Use	3
47	VS1	Module Vendor Specific 1	3
48	VccRx1	3.3V Power Supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	3
66	Reserved	For Future Use	3
67	VccTx1	3.3V power supply	2
68	Vcc2	3.3V power supply	2
69	Reserved	For Future Use	3
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Output	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Output	
76	GND	Ground	1

Module Block Diagram

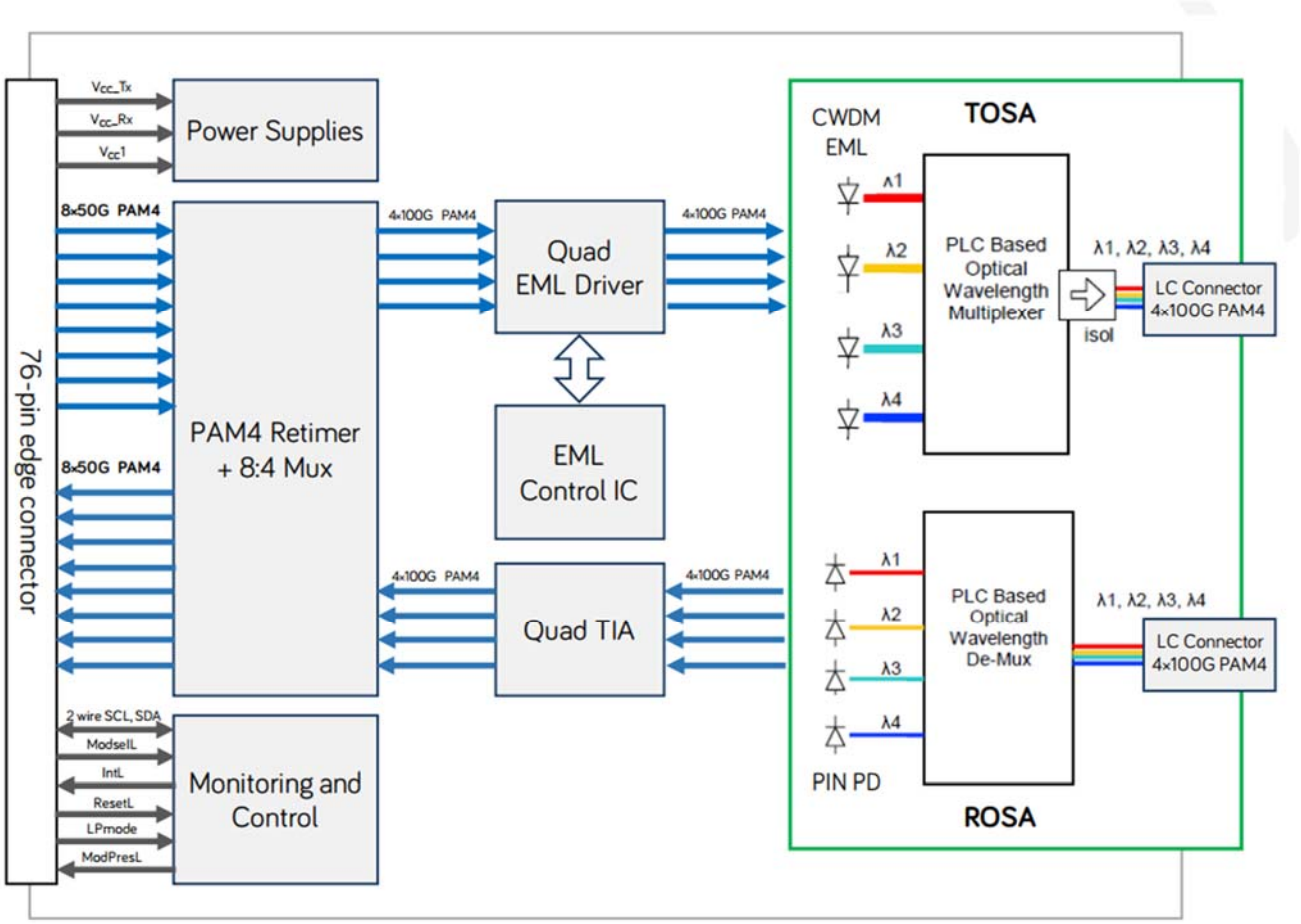


Figure 2. Module Block Diagram

Mechanical Specifications